Factsheet
InfiniBand® - SI19IB40

Silicon Cores™
Core to the Intelligent System™

Link Protocol Engine

***Silicon Interfaces'* Link Protocol Engine (LPE) is single core solution incorporating in Link Layer of Open System Interconnect (OSI) which significantly reduces the time and cost of implementing complex InfiniBand target system designs.**

InfiniBand is an open architecture interconnect solution to handle and resolve bottleneck of multiple I/O streams simultaneously. Silicon Cores proven Intellectual Property expertise for various Link Layer and experience in high--speed channel interconnect.

The SI19IB40 is a switch-based serial I/O interconnect architecture operating at a speed of 10 Gbps for 4X in each direction. The SI19IB40 transmits and receives all kind of InfiniBand packets and generates and inspects the 32-bit Invariant Cyclic Redundancy Check (ICRC) and 16-bit Variant Cyclic Redundancy Check (VCRC).

The SI19IB40 is capable of supporting unicast as well as multicast addressing. The Maximum Transfer Unit supported by the SI19IB40 is 4096 Bytes. It has four data VLs and one management VL. The flow control mechanism implemented in the SI19IB40 is separate for each data VL and it is not implemented for the management VL.

Product Specifications

- Fully synthesizable Register Transfer Level (RTL) Verilog HDL core.
- Test Bench Environment Verilog.
- Targeted FPGA Xilinx Spartan-6 / Virtex-6.
- Clock Frequency: 62.5 MHz.

Options:

(May be separately priced)

Adaptations:

√ 32-bit PCI or AMBA Host Interface Possible.

Add-ons:

√ External Link-Phy Interface Possible (for 1X/4X).

Product Highlights

- ☑ Fully compliant Infiniband architecture based on Infiniband Trade Association (IBTA) 1.0.a Specifications.
- ☑ Compliance to Test Suites as provided by University of New Hampshire Inter-Operability Lab.
- ☑ Full Duplex Independent Transmit and Receive Data Path controlled by Link State Machine.
- ☑ Optimized for the use in Host and Target Channel Adapters.
- ☑ Supports all Management and Data Packets.
- ☑ Supports all Transport Services and Raw Packets.
- ☑ Four data Virtual Lanes (VL) plus Management Virtual Lane (MVL) support.
- ☑ Provides credit based Link level flow control to handle Pipelined data.
- ☑ Has a 4X (Single Link with Receive and Transmit) physical layer independent LINK-PHY Interface
- ☑ PHY Interface Data Rate for 4X is 8 GBPS LINK-PHY; 16 GBPS for Full-Duplex
- ☑ Distinct 32-bit data lines for transmit and receive.
- ☑ Supports max up to total 512 Kbytes of external buffer memory for transmit and receive.
- ☑ External Buffer memory can be fine tuned by user as per its need of application.
- ☑ Single clock domain throughout the system.

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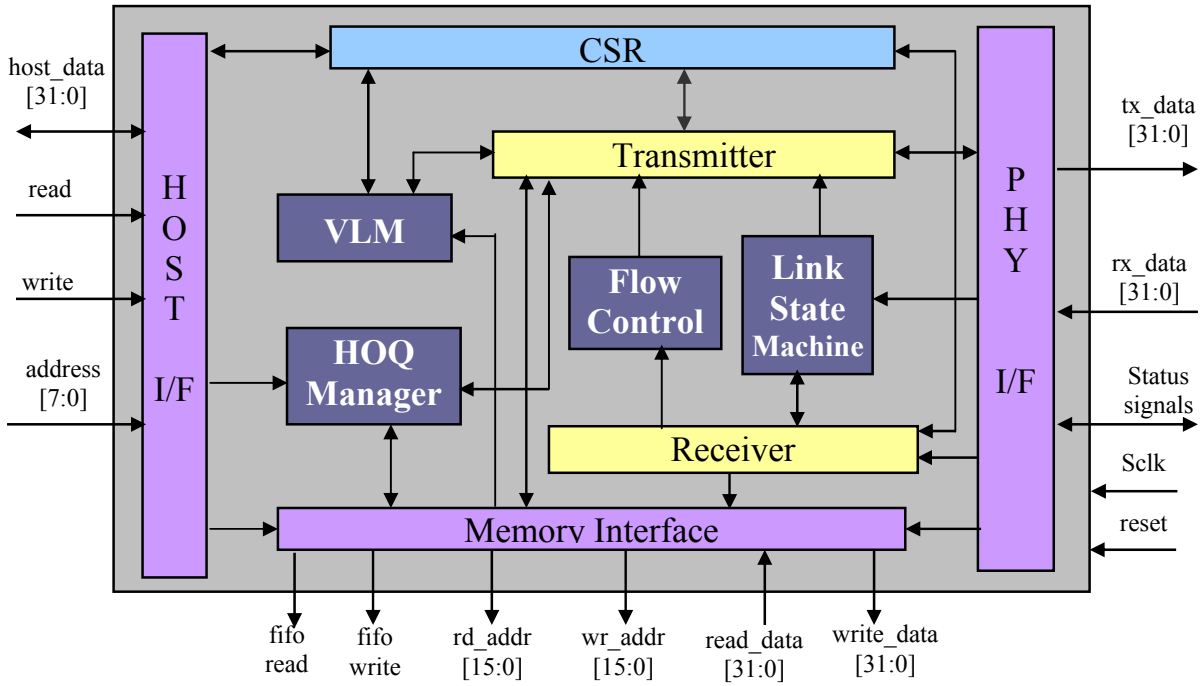
LPE Block Representative Schematic:



- Host Interface: The host Interface allows the SI19IB40 to be easily connected to the most 32 bit host processors. The host interface consists of a 32-bit data bus and an 8-bit address bus.
- Physical Interface: The physical (phy) Interface provides phy-level services to the transmitter and receiver. This includes transmission and reception of data, link and management packets and imparts status signals.
- Memory Interface: The memory Interface offers an interface to an external 512Kbytes of transmits and receives synchronous RAM. The memory allocated for each VL in the Transmit and Receive RAM is configurable.
- Control and Status Register: The Control and Status Register store the vital information desirable for the proper working of the core. It also stores the status of discarded packets while transmission and reception.
- Transmitter: The transmit retrieves data from the transmit memory and creates correctly formatted packet to be transmitted through the phy interface.
- Receiver: The receiver takes incoming data from the phy interface, checks the validity and stores the valid data into the receive memory or stores the status of the received corrupt packet into the CSR.
- Link State Machine: The Link State Machine controls the overall operation of SI19IB40. It manages the working of the transmitter and the receiver.
- Flow Control: The flow control mechanism is utilized by the IBA to prevent the loss of data packets due to buffer overflow by the receiver at each end of the link.
- VLM: The Virtual Lane Management (VLM) provides a means to implement multiple logical flows over a single physical link. The VLM is implemented according to the Infiniband Protocol.
- HOQ Manager: The Head Of Queue Manager manages the data present in the memory and discards a packet from transmission if the HOQ life has expired. The HOQ life can be configured through the CSR.

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